

PATENT APPLICATION
DOCKET NO.: 200207723-1

AMENDMENT TO THE SPECIFICATION

Please replace Paragraph [0002] with the following amended paragraph:

[0002] This application discloses subject matter related to the subject matter disclosed in the following commonly owned co-pending patent applications: following commonly owned co-pending patent applications: (i) "Programmable Clock Synchronizer," filed on 07/30/2003; Application No. 10/630,159 filed _____; Application No. _____ (Docket No. 200207722-2), in the name(s) of: Richard W. Adkisson; (ii) "System and Method for Synchronizing Multiple Synchronizer Controllers," filed on 07/30/2003; Application No. 10/629,989 filed _____; Application No. _____ (Docket No. 200207724-1), in the name(s) of: Richard W. Adkisson; (iii) "System and Method for Maintaining a Stable Synchronization State in a Programmable Clock Synchronizer," filed on 07/30/2003; Application No. 10/630,297 filed _____; Application No. _____ (Docket No. 200208008-1), in the name(s) of: Richard W. Adkisson; (iv) "System and Method for Compensating for Skew between a First Clock Signal and a Second Clock Signal," filed on 07/30/2003; Application

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No. 10/630,317 filed _____; Application No. _____
_____ (Docket No. 200208009-1), in the name(s) of: Richard W.
Adkisson; and (v) "Phase Detector for a Programmable Clock
Synchronizer," filed on 07/30/2003; Application No. 10/630,298 (now
issued as U.S. Patent No. 6,864,722) filed _____,
Application No. _____ (Docket No. 200208010-1), in the
name(s) of: Richard W. Adkisson, all of which are incorporated by
reference herein.

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Please replace Paragraph [0059] with the following amended paragraph:

[0059] Additional details regarding the various functional blocks and sub-systems described hereinabove with respect to the bus clock synchronizer controller portion and core clock synchronizer controller portion as well as the overall programable synchronizer system may be found in the following commonly owned co-pending patent applications: (i) "System and Method for Synchronizing Multiple Synchronizer Controllers," filed on 07/30/2003; Application No. 10/629,989 ~~filed _____~~, Application No. _____ (Docket No. 200207724-1), in the name(s) of: Richard W. Adkisson; (ii) "System and Method for Maintaining a Stable Synchronization State in a Programmable Clock Synchronizer," filed on 07/30/2003; Application No. 10/630,297 ~~filed _____~~, Application No. _____ (Docket No. 200208008-1), in the name(s) of: Richard W. Adkisson; (iii) "System and Method for Compensating for Skew between a First Clock Signal and a Second Clock Signal," filed on 07/30/2003; Application No. 10/630,317 ~~filed _____~~, Application No. _____ (Docket No. 200208009-1), in the name(s) of: Richard W. Adkisson; and (iv) "Phase Detector for a Programmable Clock

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Synchronizer," filed on 07/30/2003; Application No. 10/630,298 (now
issued as U.S. Patent No. 6,864,722) filed _____,
Application No. _____ (Docket No. 200208010-1), in the
name(s) of: Richard W. Adkisson, all of which are incorporated by
reference herein.